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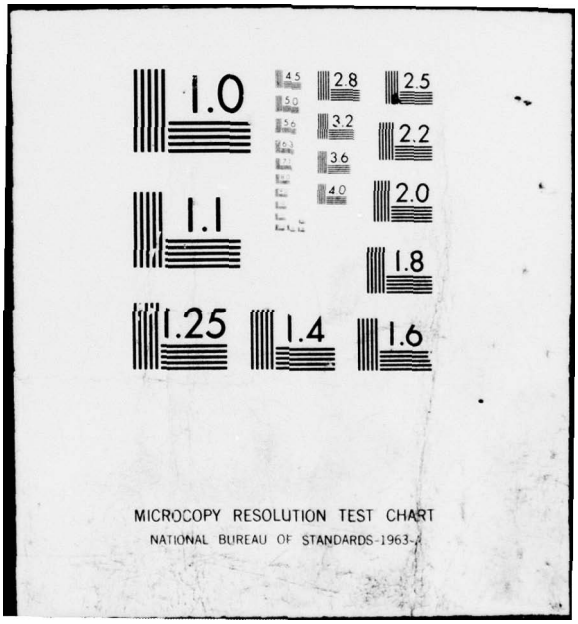
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# SOLID-STATE MODULE PHASE II

Texas Instruments Incorporated
13500 North Central Expressway
Dallas, Texas 75265

6 February 1979



Three-Month Report for Period 1 October 1978 - 31 December 1978

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This interim report covers the first three months of a six-month program to fabricate and evaluate ten X-band solid-state amplifier modules. This program is the second phase of a four-phase program to develop an all-solid-state transceiver module for use in active element, airborne array radar applications.

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The effort during this report period includes GaAs FET device fabrication with emphasis on device uniformity and yield. An improved three-stage driver amplifier has achieved an output power of 1.6 W with 20 dB gain and 29.5% power-added efficiency over the 9 to 10 GHz band. A totally integrated amplifier module housing for accommodating both the driver amplifier and the balanced output stage was also designed.

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## SECTION I
## INTRODUCTION

This interim report covers the first three months of a six-month program to assemble and evaluate ten X-band solid-state amplifier modules. This program is the second phase of a four-phase program to develop and demonstrate an all-solid-state transceiver module for use in active element, airborne array radar applications. The performance of the amplifiers was demonstrated in Phase I under Contract No. N00173-76-C-0384. An all-GaAs-FET approach was shown to be the most suitable for achieving the anticipated amplifier performance. Under the current phase, ten "baseline" power amplifier units will be assembled and evaluated for demonstration of reproducibility, repeatability of performance (unit to unit), and reliability under applicable airborne environmental conditions.

The anticipated amplifier requirements are given in Table 1. An all-GaAs-FET amplifier was selected as the optimum approach. The GaAs FET fabrication in support of the amplifier development is described in Section II of this report. The reproducibility and yield of the devices are also covered in Section II.

Section III details the design improvements on the driver amplifier and output power amplifiers. A new, integrated module housing is also discussed.

Section IV summarizes the progress made during this report period and discusses plans for the remaining three-month period of this contract.

Table 1

X-Band Solid-State Module

Amplifier Requirements

| | |
|---|---|
| Center Frequency | 9.5 GHz |
| 1 dB Bandwidth | ± 500 MHz |
| Peak rf Output | 5 W Goal, 4 W Minimum |
| Pulse Width | 2 - 20 μs |
| Duty Cycle | Up to 50% |
| Overall Gain | ≥ 25 dB |
| Final Stage Gain | 5 dB minimum |
| Risetime | < 50 ns |
| Harmonic and Spurious Output | 50 dB Down |
| Efficiency | Maximized |
| Spectral Purity | at 10 Hz -48 dB/Hz |
| | > 1000 Hz -105 dB/Hz |

## SECTION II
## GaAs FET DEVICE FABRICATION

This section discusses the device designs and process techniques chosen for this program. Device uniformity and yield that are currently being achieved are also discussed.

### A. Device Design

Devices for the last driver stage and for the balanced power amplifier are fabricated using Mask Set "g," which was designed under another program. This device design is ideal for this module in that it consists of four separate 1200 $\mu$m cells arranged in a single bar. In practice, these devices can be separated in such a way that one, two, three, or four cells are bonded as a single device. Each cell consists of eight 150 $\mu$m wide gate fingers. The gate length is 0.75 $\mu$m and is reproducibly fabricated using e-beam exposure in PMMA resist. The gate metallization is Ti/Pt/Au for reliability and ruggedness, and all active areas are protected with silicon nitride. The active layer doping concentration is 8 to 12 x $10^{16}$ $cm^{-3}$ and is thinned to a uniform and repeatable electrical thickness using anodic oxidation. The layer under the gate is thinned during processing to produce an $I_{dss}$ of 350 mA for a 1200 $\mu$m cell.

The device design and process parameters discussed here are the same as those being used to satisfy the requirements of another contract currently being performed by Texas Instruments, which requires the development of techniques for fabrication of uniform 1.5 W, 10 GHz devices. Two 1200 $\mu$m cells will satisfy that goal.

### B. Device Uniformity and Yield

Since the device design and process specifications have been fixed, considerable improvement in device uniformity has been obtained. Devices have been supplied for use on the present program from several of the 10 wafers that have been processed in

the past three months. Devices from these wafers have yielded mean values of $I_{dss}$ from 320 to 394 mA with a typical standard deviation of 8%. Problems with breakdown of the resist during plating of the bonding pads and rough mesa etching have limited the yield of complete four-cell devices to 10 to 20%, but process improvements have been made in both of these areas.

On the basis of these results, we are confident that adequate quantities of devices will be available to complete the module fabrication and that their rf parameters will be sufficiently uniform to allow operation at a common drain and gate voltage and will require minimal circuit tweaking.

## SECTION III
## AMPLIFIER FABRICATION

This section describes the circuit work performed during the first three months of Phase II of the X-band module program. Efforts during this reporting period were directed toward the design improvement of the Phase I all-FET modules. Improved matching circuits, as well as microwave performance, will be discussed. The new module housing design for the deliverable amplifiers is also described.

### A. Amplifier Configuration

The Phase II amplifier, like that of Phase I, will consist of a three-stage driver amplifier plus a balanced output stage. Figure 1 shows the GaAs FET power amplifier configuration. The driver amplifier provides 20 dB gain at 32 dBm (1.58 W) output with three cascaded FET amplifier stages. The balanced output stage is to produce 4 to 5 W output power at the 5 dB gain level.

### B. Driver Amplifier

During the early portion of this reporting period, the input/output and interstage matching networks of the driver amplifier were optimized so that little or no circuit tweaking will be required for amplifier fabrication. Because of the large number of modules required for eventual phased-array radar application, cost-effective fabrication methods are necessary design considerations.

The optimum large-signal circuit impedances for FET devices with various gate widths were determined. Figure 2 shows a Smith Chart plot of the input/output circuit impedances for FETs with 300 μm, 1200 μm, and 2400 μm gate widths, to be used in the first, second, and third stages, respectively. Based on this circuit information, new matching circuits designed for the individual stages are shown in Figure 3. With the new circuit design, output powers of 0.12 W, 0.5 W, and 1.5 W with 9 dB,

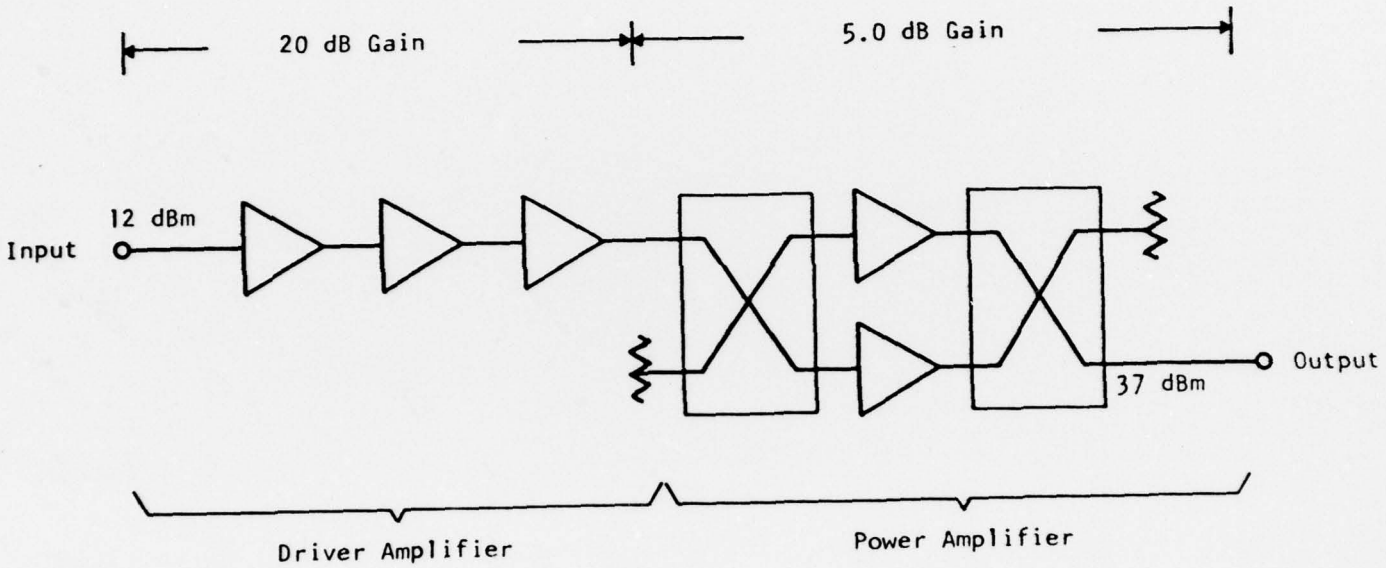



Figure 1 An All-FET Power Amplifier Configuration

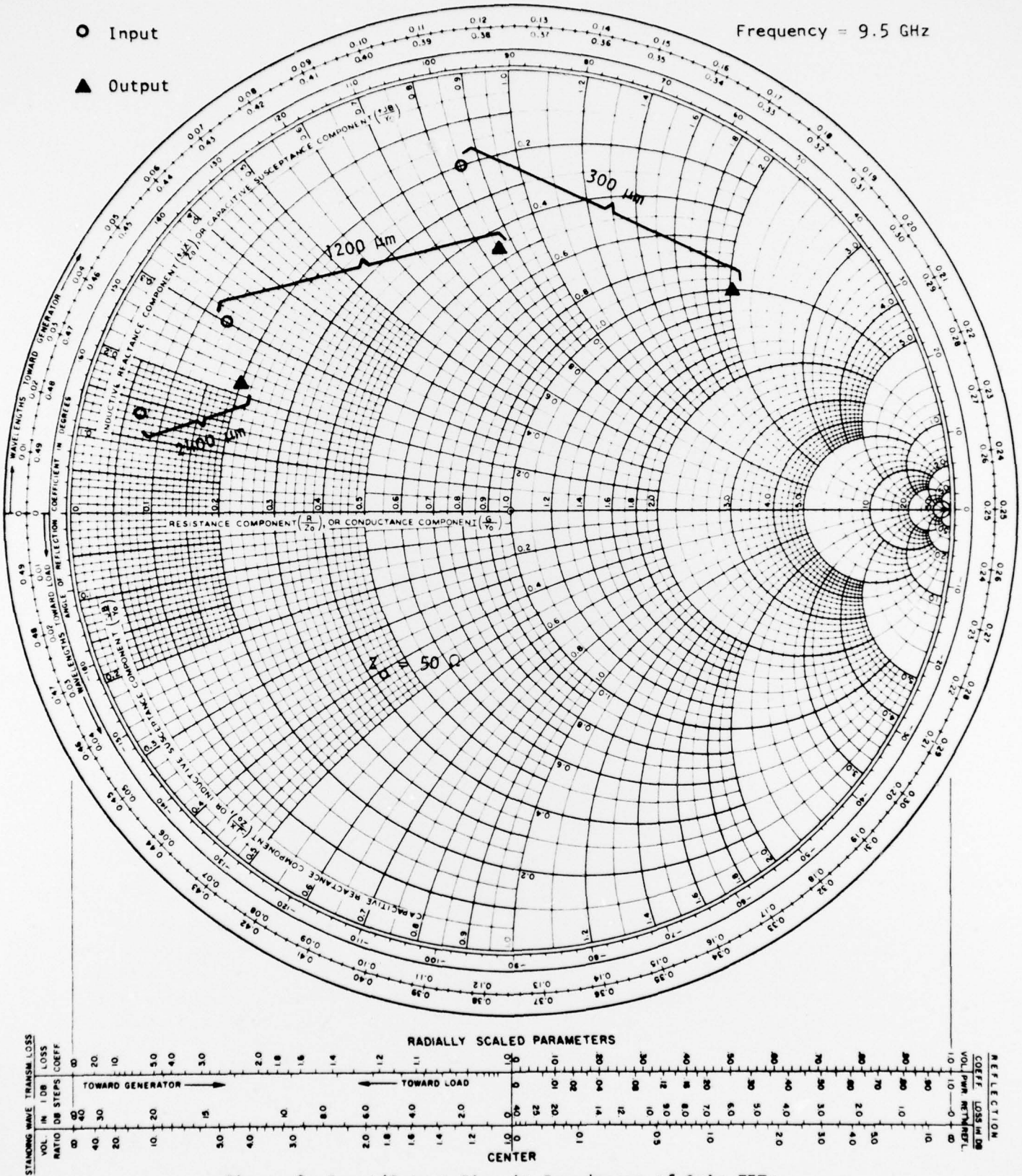
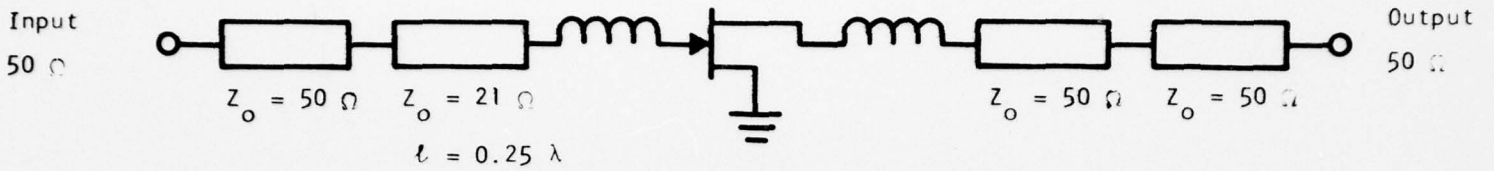
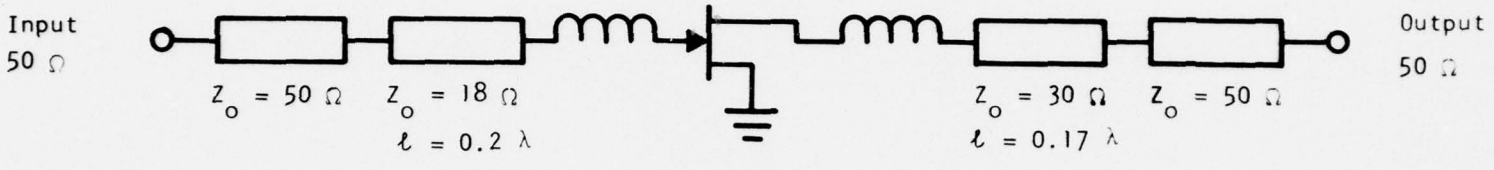



Figure 2 Input/Output Circuit Impedances of GaAs FETs



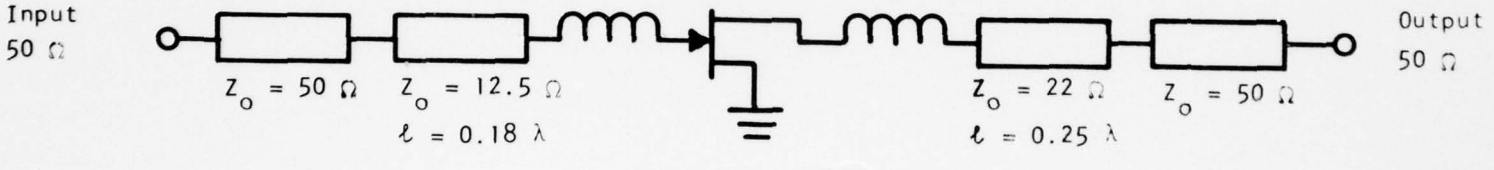

Gatewidth = 300 μm

(a)




Gatewidth = 1200 μm

(b)




Gatewidth = 2400 μm

(c)

Figure 3 Matching Circuits for the Driver Amplifier Stages
(a) First Stage (b) Second Stage (c) Third Stage
Reference Frequency for Impedance Transformers = 9.5 GHz

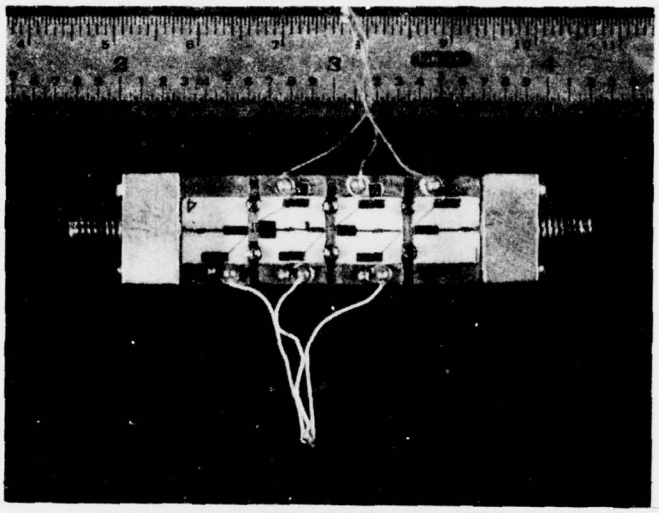
7 dB, and 5 dB of gain have been achieved for the first, second, and third stages, respectively. The 1 dB bandwidth was at least 1 GHz (9 to 10 GHz). The power-added efficiencies were in the range of 23 to 30%.

Based on the optimized circuit topologies, as shown in Figure 3, an integrated, three-stage driver amplifier with interstage impedance matching was designed, as shown in Figure 4. Like the Phase I amplifier, the devices were mounted on gold-plated copper blocks fitted to slots in the amplifier housing. Two breadboard driver amplifiers were fabricated and evaluated. Both amplifiers yield similar microwave performance. Figure 5 shows the gain-frequency response of one of these amplifiers. With + 12 dBm input, an output power of 1.6 W with 20 dB gain was obtained at 9.5 GHz. The power-added efficiency was 29.5%.

It should be noted that a single drain voltage and a single gate voltage were used for the three-stage amplifier shown in Figure 4 without using any bias networks. This design approach was aimed at simplifying the bias circuitry. A simple bias circuit is important for phased-array radar applications when thousands of amplifier modules are used. In addition to eliminating the dc power losses due to the bias networks, a single gate voltage pulse can be used to pulse-modulate all the FET stages. Since no bias network was used, a fast risetime can be achieved. Note that, even though all the drain and gate voltages were connected, unconditional stability was still obtained, as demonstrated by the fact that there was no output when the rf input power was removed. This was attributed to an effective filtering scheme used in the bias choke of the individual stages.

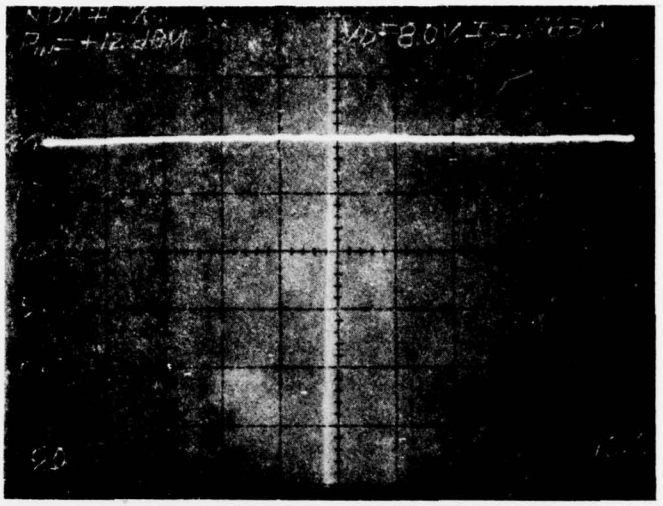
The simple bias scheme discussed above might raise the question of whether optimum amplifier performance can be achieved using devices from different slices and processing runs. It must be pointed out, however, that device design parameters such as doping levels, pinch-off voltages, etc., are essentially fixed for this

Output



Input

Figure 4 A Breadboard Three-Stage GaAs FET Driver Amplifier




$V_d$ = 8 V $I_d$ = 663 mA

$V_g$ = -1.5 V

Efficiency = 29.5%

rf Input = +12 dBm

Figure 5 Performance of a Three-Stage FET Driver Amplifier

particular module application (see Section II). Any devices with unacceptable parameter deviations will be precluded from use in the module. Experimental results obtained so far indicate that, with the present device design, the optimum drain voltage will be in the range of 8 to 9 V, while the optimum gate voltage will be in the -1 to -1.5 V range.

The three-stage driver amplifiers described above were also pulse-operated. The gate voltage was used to pulse-modulate the amplifier. A risetime of $\sim$ 30 ns has been achieved for the driver amplifier. A 275 pF chip capacitor was used in shunt with the bias choke of each stage.

## C. Output Amplifier Stage

After completion of the three-stage driver amplifier design, as discussed above, the circuit effort was directed toward the 5 W FET output stage development. A balanced amplifier configuration was used. A 3 dB Lange-type coupler on a 0.015 inch quartz substrate was designed and fabricated. This coupler has essentially the same dimensions for the coupling section as those used in the Phase I amplifier, except that the input/output 50 $\Omega$ lines have been modified to fit into the new housing (see Section III.D).

To efficiently combine several cells, a lumped element impedance matching approach was used, as in the output stage of the Phase I amplifier. The basic circuit topology is shown in Figure 6. The values of the input/output matching capacitors are shown. It was demonstrated in Phase I that an output power of 2 to 2.5 W with 5 to 6 dB gain can be obtained with this impedance matching technique at X-band. A four-cell (4800 $\mu$m gate width) FET was used. For the Phase I amplifier, shunt capacitors were used for the input and output of each of the transistor cells. As a result, a total of eight chip capacitors was needed for a four-cell amplifier. For the Phase II program, the possibility of using fewer matching capacitors was explored. It has been shown recently that two cells (2400 $\mu$m gate width) can share

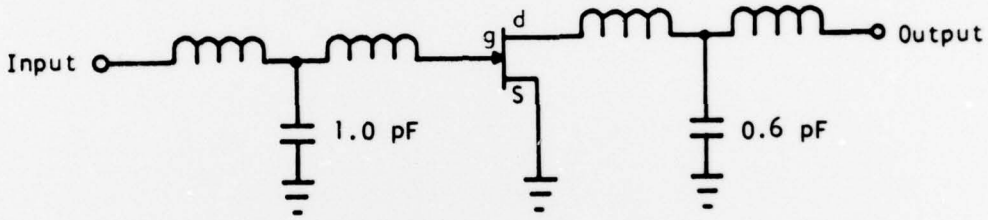


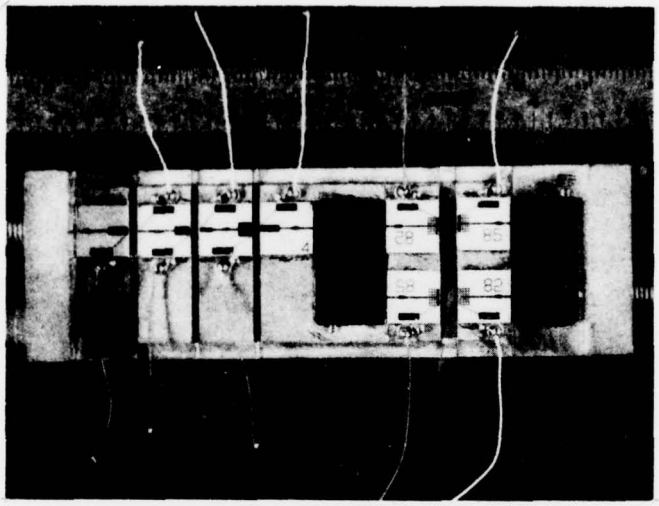

Figure 6 Circuit Topology for Matching GaAs FET With Lumped LC Elements

a common shunt input capacitor (1 pF) and a common output capacitor (0.5 pF). Therefore, only four MOS capacitor chips will be required. With this new matching configuration, an output power of 2 W with at least 5 dB gain can generally be obtained for the four-cell amplifier. The element values are still being optimized for higher cell-combining efficiency. Two such four-cell amplifier stages will be combined in a balanced configuration in the integrated power amplifier.

## D. Amplifier Module Integration

Concurrent with the amplifier design effort discussed in Sections III.A through C was the task to redesign the module housing for the Phase II program. An integrated module housing (Figure 7) was chosen as the design approach. Note that the devices were not mounted. This mechanical configuration eliminates potential problem areas such as ground-plane discontinuity, connector-circuit interface, etc. The price paid for such an integrated approach is that the driver amplifier and the output balanced amplifier cannot be checked separately prior to cascading. However, with the optimized circuit topologies as outlined above, little tweaking will be necessary. The module shown in Figure 7 has dimensions of 8.4 cm x 3.0 cm x 1.5 cm (3.3 inch x 1.2 inch x 0.6 inch). A three-stage, single-ended driver amplifier and a balanced output stage are accommodated. In addition to the input/output OSM connectors, a multipin connector for the dc and pulse bias is also provided.

Input



Output

Figure 7 A Phase II Solid-State Amplifier Module

## SECTION IV
## SUMMARY AND PLANS

During the first three months of this Phase II program, the design and process specifications for the necessary devices have been identified. The uniformity and repeatability of devices fabricated since those specifications were fixed have been encouraging. An improved three-stage driver amplifier was designed and fabricated. With essentially no circuit tweaking required, an output power of 1.6 W with 20 dB gain and 29.5% power-added efficiency were achieved.

Plans for the remaining three-month period of the contract include continued device process improvement, fabrication of devices as required for amplifier assembly, completion of the balanced output stage design, and assembly and testing of the ten amplifier modules for delivery.